layers. The N- layer in Beasom '153 is a very low dopant layer therefore having the N-notation. The P region 36 in Beasom '153 is a generally medium dopant region compared to the N+ region 34. Region 34 is the only highly dopant buried region in Beasom '153 which has no contact with the upper surface.

To avoid any confusion applicant has amended the claims to indicate that the buried regions are specifically N+ and P+ and therefore a highly dopant region as compared to the remaining layers and regions formed therein to constitute the active devices. It should be noted that it is well known in the art of semi-conductor fabrication that a "buried" layer process includes a heavily dopant N+ type region. Attached is a treatise of Integrated Circuits, Designed Principles and Fabrication (c)1965 p.189 to associating the meaning of the term "buried" and N+ layer.

Thus the Beasom U.S. Patent 5,652,153 does not anticipate the limitation of claim 1, since it does not have a unselective N+ buried layer and it does not have a selectively formed P+ buried layer. Nor would it be obvious to modify it with Parker et al. nor Pendharkar et al. The other independent claims and the dependent claims are allowable for the same reason as well as their additional limitations.

It should be noted that claim 18 is not rejected in the body of the office action.

Upon review of the above arguments it will be evident that the present application that claims 1-39 and 57-64 are allowable over the art of record.

The non-elected claims have been cancelled with no intent to abandon, it will be the subject of future applications. The present application is considered in condition for allowance and thus passage to issue is hereby requested. A favorable examination of the subject application is hereby requested.

Respectfully submitted,

BARNES & THORNBURG LLP

Perry Palan

Reg. No. 26,213

(202) 289-1313

Enclosure

INTEGRATED CIRCUITS

Design Principles and Fabrication

OTOROLA INC.

EDITOR

Raymond M. Warner, Jr.

DIRECTOR OF ENGINEERING MOTOROLA INC., SEMICONDUCTOR PRODUCTS DIVISION

ASSOCIATE EDITOR

James N. Fordemwalt

PROJECT MANAGER
MOTOROLA INC., SEMICONDUCTOR PRODUCTS DIVISION

RADIATION, Inc. Melbourne, Florida

ASSISTANT EDITORS

Charles S. Meyer David K. Lynn Michael J. Callahan Lothar Stern

MCGRAW-HILL BOOK COMPANY

New York

San Francisco

Toronto

London

Sydney

Copyright © 1965 by Motorola Inc., Semiconductor Products Division. All Rights Reserved. Printed in the United States of America. The contents of this book are based on Integrated Circuits Design courses given by Motorola Inc. Motorola Inc. has patent coverage on some subject matter in the present book, and is seeking patent coverage on other subject matter herein. There is no direct or implied license from Motorola Inc. under patents or patent applications of Motorola Inc. or any other company. In the absence of written agreement to the contrary, Motorola Inc. assumes no liability for patent infringement arising out of any use of the subject matter of this book. Reproduction in whole or part forbidden without permission of Motorola Inc., Semiconductor Products Division. Library of Congress Catalog Card Number: 64-22197

43525

5 6 7 8 9 10 11 12 - MAMB - 7543210698

e of each

(7-23)

ween the

(7-24)

(7-25)

(7-26)

ransistor, or, where vering the series refact that e doublel become from the

nonolithic tage drop the junc-'olt for an

siderably .075 volt. cause the ion-gold-

(7-27)

s a total of 2 less

(7-21), is on-goldler α_i , its

If a higher level of current operation is required, then by scaling up the geometry to a 1- by 6-mil structure, for example, the series resistance can be reduced even further. For an emitter length of 6 mils,

$$\bar{l} = \frac{1}{2}(l_E + l_C) = \frac{1}{2}(6 + 9) = 7.5 \text{ mils}$$
 (7-28)

and

$$r_{SC} \approx \frac{0.1 \text{ ohm cm} \times 2 \text{ mils}}{2 \times 7.5 \text{ mils} \times 22 \times 10^{-4} \text{ cm}} = 6 \text{ ohms}$$
 (7-29)

Thus, the scaling up of the geometry reduces the series resistance from about 15 to 6 ohms.

If we saturate the gold-doped transistor at a collector current level of 20 mA and an I_C/I_B ratio of 10, then we obtain the same junction potential V_{CE} as given by Eq. (7-27). The series voltage drop at 20 mA through 6 ohms would equal 0.12 volt. Therefore, the total $V_{CE(SAT)}$ for the 1- by 6-mil gold-doped monolithic transistor at 20 mA is 0.31 volt.

One useful method of reducing the collector series resistance of a monolithic transistor is illustrated in Fig. 7-10. This is the so-called "buried" layer process by

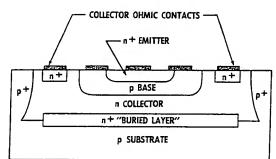


Fig. 7-10 Use of a "buried" n⁺ layer to reduce collector series resistance.

which a heavily doped n^+ -type region is sandwiched between the n-type epitaxial collector and the p-type substrate. This buried n^+ region has the effect of shunting the high-resistivity collector region, thereby reducing the series resistance considerably. There are two basic methods of achieving this particular structure, namely, (1) by diffusing the n^+ layer into the p-type substrate before the growth of the n-type epitaxial collector, and (2) by selectively growing the n^+ regions, using masked epitaxial techniques, and then continuing on by growing the n-type collectors epitaxially. This technique results in nearly an order of magnitude reduction in r_{SC} . The striking advantage of the buried layer structure is that for saturated switching transistors we can now design on the basis of higher resistivities for the collector region, in order to reduce capacitance and still obtain very low r_{SC} .

7-7 Frequency Response of Monolithic Transistors

The frequency response of a monolithic transistor is best characterized by the parameter f_T , which is that frequency at which the magnitude of β is equal to unity